



AO4480

N-Channel Enhancement Mode Field Effect Transistor



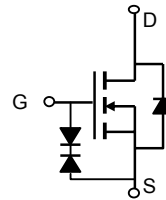
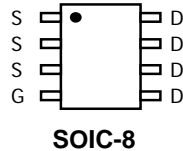
General Description

The AO4480 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It is ESD Protected. This device is suitable for use as a low side switch in SMPS and general purpose applications. *Standard Product AO4480 is Pb-free (meets ROHS & Sony 259 specifications).*

Features

V_{DS} (V) = 40V
 I_D = 14A (V_{GS} = 10V)
 $R_{DS(ON)} < 11.5m\Omega$ (V_{GS} = 10V)
 $R_{DS(ON)} < 15.5m\Omega$ (V_{GS} = 4.5V)
 ESD Rating: 4KV HBM

UIS Tested
Rg,Ciss,Coss,Crss Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^{AF}	I_{DSM}	$T_A=25^\circ\text{C}$	14
		$T_A=70^\circ\text{C}$	11
Pulsed Drain Current ^B	I_{DM}	70	A
Power Dissipation	P_D	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2.0
Avalanche Current ^B	I_{AR}	30	A
Repetitive avalanche energy 0.3mH ^B	E_{AR}	135	mJ
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	30	40	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^A		Steady-State	59	75
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	16	24	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=32\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1	uA
					5	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$			± 100	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	1	2	3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=10\text{V}$, $V_{DS}=5\text{V}$	70			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=10\text{V}$, $I_D=14\text{A}$ $T_J=125^\circ\text{C}$		9	11.5	m Ω
				13		
					12	15.5
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=14\text{A}$		50		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.7	1	V
I_S	Maximum Body-Diode Continuous Current				4	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance			1600	1920	pF
C_{oss}	Output Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=20\text{V}$, $f=1\text{MHz}$		320		pF
C_{rss}	Reverse Transfer Capacitance			100		pF
R_g	Gate resistance	$V_{GS}=0\text{V}$, $V_{DS}=0\text{V}$, $f=1\text{MHz}$		3.4		Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $I_D=14\text{A}$		22		nC
$Q_g(4.5\text{V})$	Total Gate Charge			10.5		nC
Q_{gs}	Gate Source Charge			4.2		nC
Q_{gd}	Gate Drain Charge			4.8		nC
$t_{D(on)}$	Turn-On Delay Time			3.5		ns
t_r	Turn-On Rise Time	$V_{GS}=10\text{V}$, $V_{DS}=20\text{V}$, $R_L=1.5\Omega$, $R_{GEN}=3\Omega$		6		ns
$t_{D(off)}$	Turn-Off Delay Time			13.2		ns
t_f	Turn-Off Fall Time			3.5		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=14\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		31		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=14\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$		33		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

F: The current rating is based on the $\leq 10\text{s}$ junction to ambient thermal resistance rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

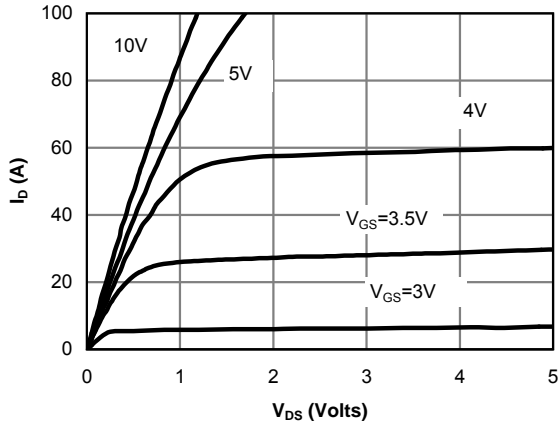


Figure 1: On-Region Characteristics

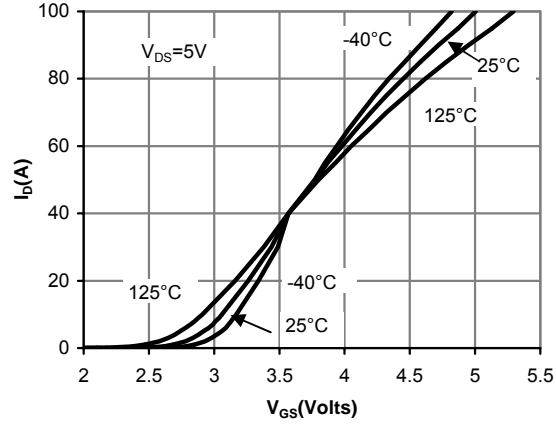


Figure 2: Transfer Characteristics

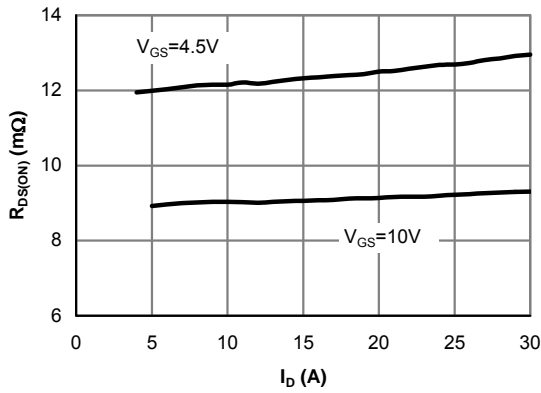


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

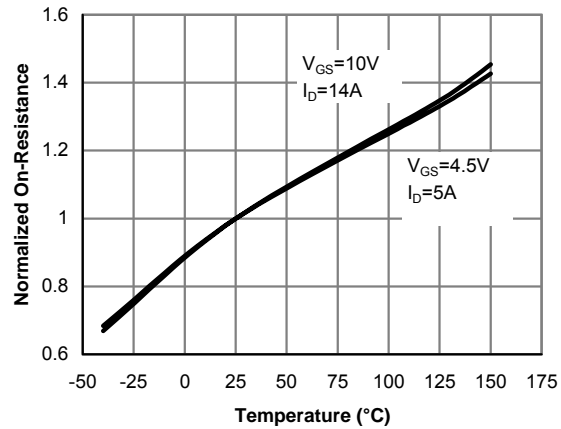


Figure 4: On-Resistance vs. Junction Temperature

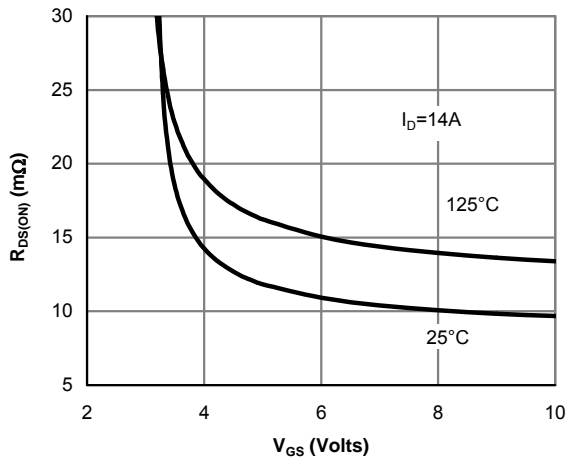


Figure 5: On-Resistance vs. Gate-Source Voltage

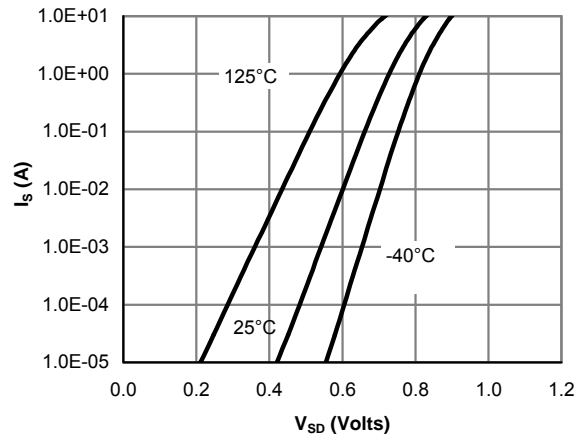


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

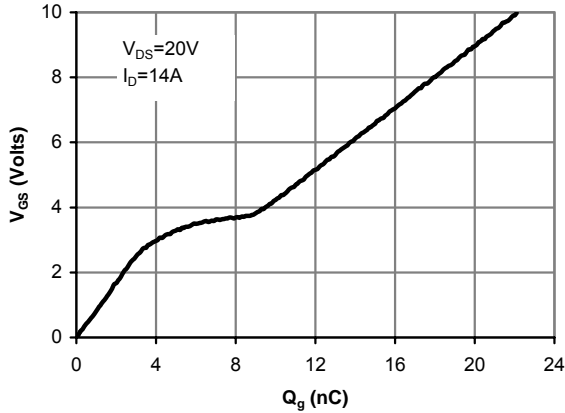


Figure 7: Gate-Charge Characteristics

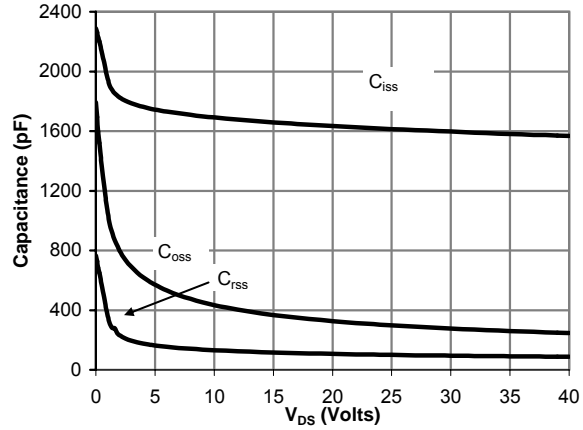


Figure 8: Capacitance Characteristics

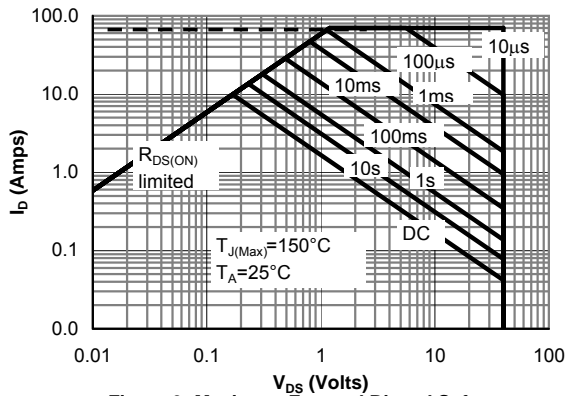


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

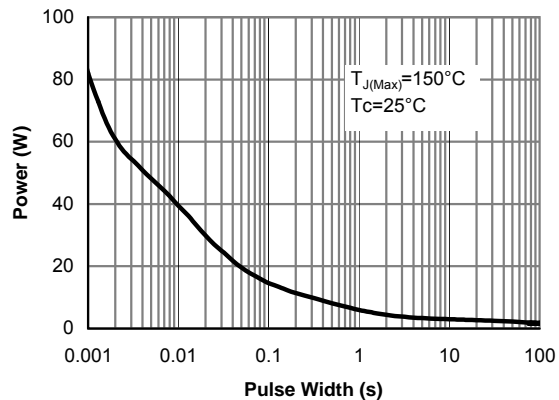


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

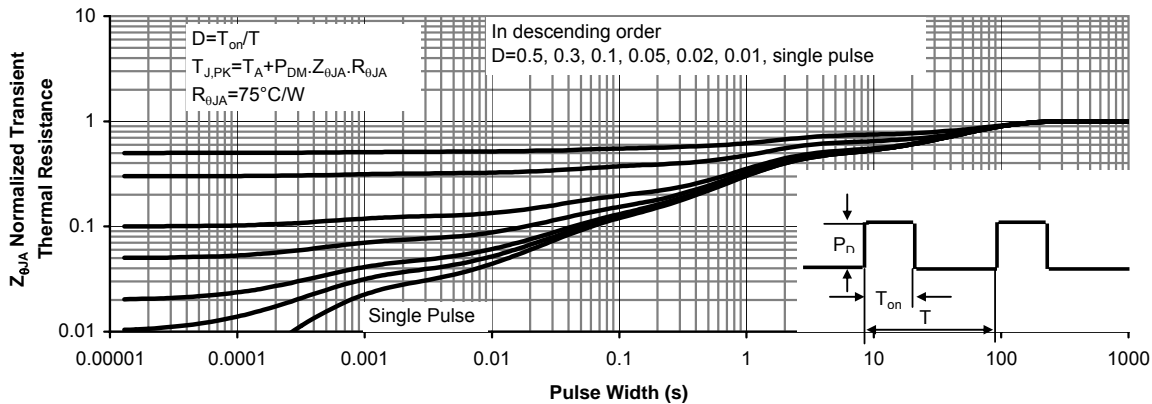


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)